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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/553,470	05/19/2006	Ralf Lerner	60291.000041	8935

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EXAMINER	
LOPEZ ESQUERRA, ANDRES	
ART UNIT	**PAPER NUMBER**
2818	

MAIL DATE	DELIVERY MODE
07/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/553,470	LERNER, RALF	
	Examiner	Art Unit	
	ANDRES LOPEZ ESQUERRA	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *27 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 27, 2008 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1 – 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsiao et al. US 6,515,826 (Hsiao) in view of So US 6,242,320 (So), and further in view of Hartmannsgruber, et al., "A Selective CMP Process for Stacked low-k'CVD Oxide Films", Microelectronic Engineering, Vol. 50, pg. 53-58, 2000 (Hartmannsgruber).**

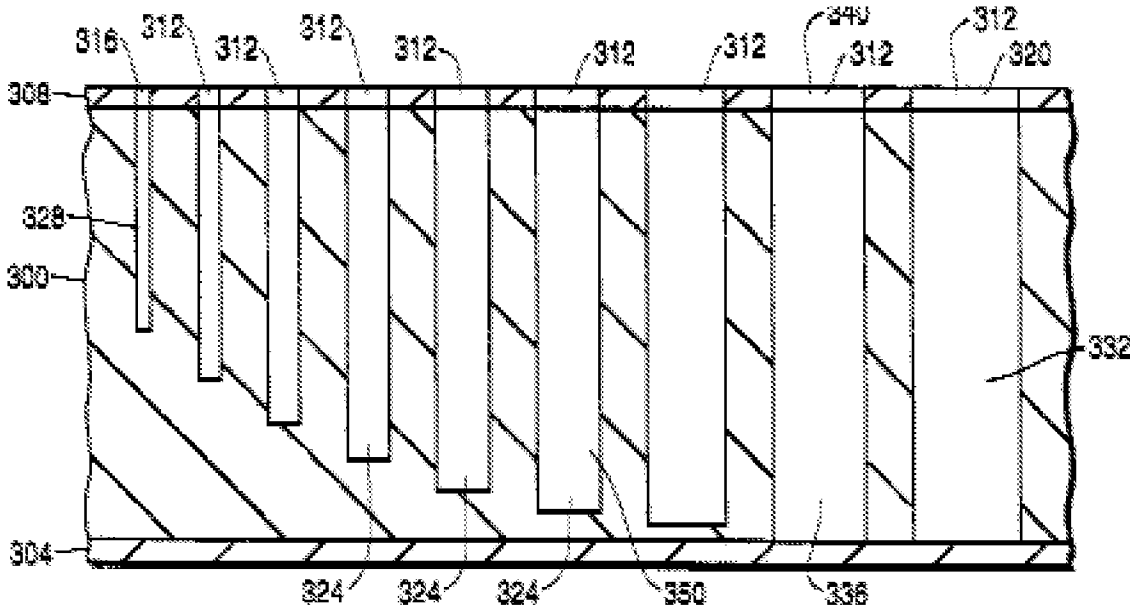


FIG.15

4. As for claims 1 – 3, 5 – 6, 9 – 10, 14, 17, 20 and 24, Hsiao discloses (Col 6 line 36 – Col 8 line 24) and shows in Fig 15 a device and method of manufacturing a semiconductor structure utilizing aspect ratio dependent etching comprising:

a. forming a test structure (Fig 15), defined by a systematic row of a plurality of trenches (324, 328, 336) having different widths and different depths in a defined manner, in an active wafer (300), said wafer receiving an active circuit (148, 178, 198, 222, 202) in a later stage;

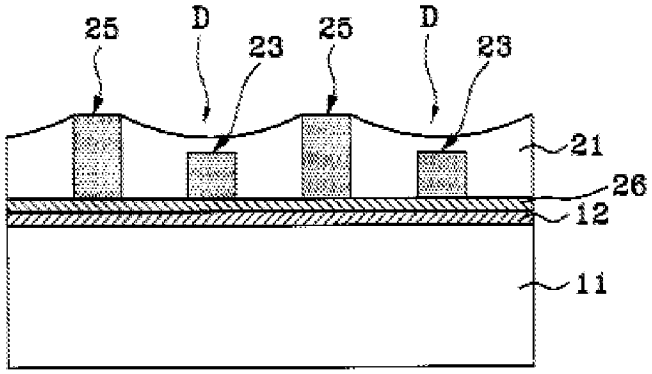
i. wherein the deep trenches are formed in a etch process using an etch mask (308) having openings of different widths for the trenches of different widths (Claim 2 – 3);

b. wherein a targeted thickness of the active wafer (2) during the removal corresponds to a depth of a reference trench (350) of the trenches of the test structure, said reference trench (350) being flanked by shallower and deeper

trenches, in particular by a neighboring shallower and a neighboring deeper trench (328,336);

5. Hsiao fails to teach the bonding of a carrier wafer after creating the trenches and the use of a polishing process on the backside of the active wafer made of silicon until exposing the reference trench.

FIG.2G



6. So discloses (Col 2 line 66 – Col 4 line 51) and shows in Fig. 2A – 2I a device and a method of manufacturing a semiconductor wafer comprising:

c. forming a structure in an active wafer made of a silicon wafer (21) with a plurality of different trenches with different depths (22,24) including a reference trench (24);

d. performing the wafer material removal process comprising a polishing process, commencing from the backside of the active wafer (21) until the reference trench (24) is exposed;

ii. wherein the polishing process is interrupted at least once (So discloses a two step polishing process (Col 4 lines 9 – 30)) (Claim 9 and 14).

e. bonding the active wafer (21) with a side, in which the test structure is formed, onto the second wafer of the semiconductor wafer pair, in particular onto a second wafer (applicant's carrier wafer claim 17) (30) comprising silicon and oxide layers, and;

f. forming an active circuit in said active wafer in said later step (Col. 4, lines 25 – 27).

7. So is evidence that ordinary workers in the art would find a reason, suggestion or motivation to use bond the active wafer made of silicon after creating the trenches to a carrier wafer and performing a polishing process in steps until exposing the reference trench.

8. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Hsiao by using bond the active wafer made of silicon after creating the trenches to a carrier wafer and performing a polishing process in steps until exposing the reference trench for advantages such as having a uniform semiconductor layer in the active wafer so as to have a better surface for the future device to be form as well as having better characteristics of the overall device (Col 2 lines 7 – 24).

9. Hsiao in view of So still fails to disclose the use of an optical device in the process (claim 1, 9 – 10 and 14)

10. Hartmanngruber discloses (Page 53 – 54) a selective CMP process in a semiconductor substrate using the materials of silicon and silicon dioxide that uses a Tencor α–step profilometer (applicant's optical device) to measure the topography of the surface.

11. Hartmannsgruber is evidence that ordinary workers in the art would find a reason, suggestion or motivation to use a Tencor α–step profilometer (applicant's optical device) to measure the topography of the surface on a semiconductor substrate using the materials of silicon and silicon dioxide during a selective CMP process to terminate the polishing process.

12. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Hsiao in view of So by using a Tencor α–step profilometer (applicant's optical device) to measure the topography of the surface on a semiconductor substrate using the materials of silicon and silicon dioxide during the selective CMP process to terminate the polishing process for advantages such as having a uniform semiconductor layer in the active wafer so as to have a better surface for the future device to be form as well as having better characteristics of the overall device (So Col 2 lines 7 – 24).

13. Also, as for the limitation of "said active wafer provided for receiving an active circuit in a later step" (claim 1) recitation of the claimed invention does not result in a structural difference between the claimed invention and the prior art, thus claimed invention is only an art recognized suitability for an intended purpose, MPEP 2144.07.

14. Furthermore, as for the limitation of claim 22 – 23 of the use of silicon and silicon dioxide, Hsiao discloses the claimed invention except for the use of silicon and silicon dioxide for the specific different wafers. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to use of silicon and silicon dioxide for the different wafers, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

15. Also, as for claim 10 limitation of "a thickness of the active wafer correspond to a depth of a reference trench of the test structure as targeted thickness during a removal process from the backside of the active wafer until the reference trench and the bottom of the reference was exposed" is considered as a product by process limitation. "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even thought the prior product was made by a different process." In re Thorpe, 777F, 2d 659, 698, 227 USPQ 964, 966 (Fed. Cir. 1985); see also MPEP 2113.

16. Finally, a recitation of " said first wafer for receiving an active circuit in a later stage" and "for monitoring the reduction in thickness" of the claimed invention does not result in a structural difference between the claimed invention and the prior art, thus claimed invention is only an art recognized suitability for an intended purpose, MPEP 2144.07.

17. As for claims 4, 11, and 21, Hsiao shows in Fig 15 the trenches are open and un fill.

18. As for claims 7 – 8, 12 – 13, 15 – 16, and 18 - 19, Hsiao discloses (Col 6 line 59 – Col 7 line 31) and shows in Fig. 15 the composition of the trenches to be a series of stripe-like shape trenches which are parallel in a continuously shallower or deeper series with increasing widths openings, wherein the trenches are more broader the more deeply they are formed. Also, Hsiao discloses (Col 6 line 59 – Col 7 line 50) and shows in Fig. 15 that the reference trench (350) (applicant's predefined target thickness) Is located in a central region of the structure with trenches on one side with openings of smaller width and smaller depth and trenches on the other side with openings of greater width and greater depth. and that depth increases as the corresponding width increases in the structure

Response to Arguments

19. Examiner would like to point out that if applicant's next amendment further defines the claimed invention in more detail in such a way that the method and device are more distinct, a restriction might be in order for the case.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6,156,621 and US 6,514,858.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANDRES LOPEZ ESQUERRA whose telephone number is (571)272-9753. The examiner can normally be reached on M - Th 6:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven H. Loke can be reached on (571) 272 - 1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrés López-Esquerra
Examiner
Art Unit 2818

ALE

/DAVID VU/
Primary Examiner, Art Unit 2818